Aung Pyae (Earnest) Phyo

(510)-449-9834 | earnest.lin@outlook.com | www.linkedin.com/in/earnestlin
Portfolio - earnestl.github.io/Portfolio_Website

Education

University of California, Berkeley Berkeley, CA
B.S Electrical Engineering and Computer Science *Expected Graduation: 12/2025*
Relevant Coursework: *Data Structures & Algorithms, Discrete Mathematics & Probability, Computer Architecture, Digital Design & Integrated Circuits*

Technical Skills

Languages/Frameworks: C, C++, Python, SQL, HTML/CSS, Java/TypeScript, React, Assembly, FastAPI, Verilog
Tools: Git, GDB, AWS, DigitalOcean, Docker, Supabase, Numpy, RISC-V, KiCAD, Logisim, Arduino, FPGA, PIC

Experience

Software Engineer 06/2024 - Present
Kaylie.ai *CA*
- Built backend REST API with FASTAPI for the initiation and monitoring of Insurance verification instances
- Designed PostgreSQL database schemas for Insurance verification dashboard, ensuring the integration of various external web services/automation to process and visualize relevant data
- Implemented CI/CD pipeline using Github actions to unit test and automate the dockerization and the deployment of internal APIs from Docker Hub to DigitalOcean
- Designed and implemented a secure solution for the storage and retrieval of confidential third-party information by utilizing 1Password's Connect server, Fastapi, and PyCryptodome
- Incorporated JSON/data parsing, management, and visualization from file uploads by leveraging a data ingestion service and a workflow orchestration platform enabled with YAML configurations to streamline data transparency

MPLS Lab Technician 03/2023 - 10/2023
Genentech *San Francisco, CA*
- Operated ovens, washers, and autoclaves in accordance with non-impact GMP regulations
- Progressed in continuous improvements utilizing Lean methodologies
- Reassessed and/or put together IPs and OJTs for an in-progress Centralized Services team

Equipment Maintenance Engineer Intern 06/2022 - 09/2022
Tesla *Fremont, CA*
- Established and optimized preventive maintenance procedures that benchmarked up to x9 the efficiency
- Sorted and documented parts of 10+ obsolete machines to be repurposed as spares for those in current use
- Commenced implementation of a temperature monitoring system in power cabinets through which programmed alarms will be incorporated and data for adequate cooling will be yielded

Projects

RISC-V CPU with Audio Synthesizer | *Verilog, RTL Design, UART* 08/2024 - Present
- Implemented a 3-stage pipelined RISC-V CPU using Verilog, targeting Xilinx PYNQ-Z1 platform
- Integrated UART for tethering and IO/audio components, building a simple audio synthesizer from lab modules
- Mapped high-level specs to RTL design, resolving hazards in a pipelined architecture
- Developed BIOS for instruction execution and successful memory management

Tamagotchi Battler | *C++, ESP32, Arduino, SPI, I2C, FreeRTOS operating system* 05/2024
- Designed and built firmware for an ESP32-based hand-held device that emulates a digital pet which the user is responsible for taking care of and with which multiple users can engage with each other in a form of a battle.
- Employed multi-threaded application using FreeRTOS to achieve reliable execution of tasks, low latency interrupts management, and seamless animation display of multiple elements on the screen
- Established peer-to-peer network across authenticated ESP32 to enable secure communication for battling function

Digitized Record Player Replica | *C, PIC, KiCAD, Arduino* 08/2023
- Designed schematic of record player replica which plays digitized music from an sd card
- Programmed PIC mcu based embedded system and employed a variety of technologies such as PWM, UART, & comparators to interface with external devices